

IN THE CLAIMS

Please add the following new claims:

*Sub C1* ~~61.~~ A non-volatile memory circuit, comprising:

a plurality of memory cells each comprising a ferroelectric capacitor connected in series with an access transistor between a plurality of respective drive lines and a common bit line,

5 a plurality of word lines connected respectively to control terminals for a plurality of said access transistors for activating respective ones of said access transistors upon receipt of a selection signal for one of said memory cells, and

10 a differential sense amplifier for reading from and writing to said memory cells, said sense amplifier having a first input connected to said bit line, and a second input connected to receive a reference signal, said sense amplifier having a data input/output terminal, said sense amplifier for differentially driving said first and second input lines for reading a data

15 state from one of said memory cells connected thereto and for applying the data state thus read to said input/output terminal, and said sense amplifier for driving said bit lines connected to said selected memory cell to one of a set of predetermined voltage states corresponding to a data state received at said

20 input/output terminal for writing said received data state into the selected one of said memory cells.

*B3* ~~62.~~ A non-volatile memory circuit as recited in claim 61 wherein said reference signal is a predetermined voltage.

*Sub C2* ~~63.~~ A non-volatile memory circuit as recited in claim 61 including a respective complementary memory cell for each of said plurality of memory cells wherein the output of the corresponding complementary memory cell is transmitted through a bit line to provide said reference signal to said sense amplifier.

64. A non-volatile memory circuit as recited in claim 61 including multiple sets of said memory cells, each set having a respective common bit line thereby forming a memory circuit matrix comprising rows and columns of said memory cells. *✓✓*

65. A non-volatile memory circuit as recited in claim 61 including means for isolating said sense amplifier from said bit line. *✓✓*

*b* 3 *D* 66. A non-volatile memory cell as recited in claim 61 including a dummy ferroelectric capacitor memory cell for said plurality of memory cells and a bit line connected to provide the output of the dummy memory cell as the reference signal to said sense amplifier. *✓✓*

5 2967. A non-volatile memory circuit, comprising:  
a plurality of memory cells each comprising a  
ferroelectric capacitor connected in series with an access  
transistor between a plurality of respective bit lines and a  
common drive line,

a word line connected to control terminals of said access  
transistors for activating said transistors upon receipt of a  
selection signal for one of said memory cells, and

10 a plurality of differential sense amplifiers corresponding  
respectively to said bit lines for reading from and writing to  
said memory cells, each sense amplifiers having a first input  
connected to the corresponding bit line and a second input  
connected to receive a reference signal, each said sense  
amplifier having a data input/output terminal, said sense  
15 amplifiers for differentially driving said first and second  
inputs thereof for reading a data state from the one of said  
memory cells connected thereto, and for applying the data state  
then read to said input/output terminal, and said sense  
amplifiers for driving the corresponding bit lines connected to  
20 said memory cells to predetermined voltage states corresponding  
to a data state received at said input/output terminal for  
writing said received data state into the corresponding one of  
said memory cells.

2968. A non-volatile memory circuit as recited in claim 67  
wherein said reference signal is a predetermined voltage.

*Surf C* 2969. A non-volatile memory circuit as recited in claim 67  
including a respective complementary memory cell for each of said  
plurality of memory cells wherein the output of the corresponding  
complementary memory cell for each of said plurality of memory  
5 cells wherein the output of the corresponding complementary  
memory cell is transferred through a bit line to provide said  
reference signal to the second input of the corresponding sense  
amplifier.